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Richard Raimi , Jacob Abraham
Proceedings of the 36th ACM/IEEE conference on Design automation conference June 1999 | 82% |
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A well-known problem in timing verification of VLSI circuits using static timing analysis tools is the generation of false timing paths. This leads to a pessimistic estimation of the processor speed and wasted engineering effort spent optimizing unsensitizable paths. Earlier results have shown how ATPG techniques can be used to identify false paths efficiently [6],[9], as well as how to bridge the gap between the physical design on which the static timing analysis is based and the test view on w ... | 77% |

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